REMARKS

This amendment responds to the office action mailed January 20, 2004. In the office action the Examiner:

- rejected claims 1-9, 13-14, 16-22 under 35 U.S.C. 103(a) as being unpatentable over Cheney (US 5,668,599) in view of Smith (US 5,802,600).

Claim 13 recites a computer readable memory that directs a computer to function in a specified manner. The memory comprises a buffer management module to establish at least two distinct buffer sizes for a scalable buffer in the memory, a video decoding module to process a video stream with the scalable buffer configured to the two respective buffer sizes and an analysis module to monitor the computer's corresponding cache memory performance, e.g., cache miss rate, associated with the two separate processes of the video stream by the video decoding module. The analysis module includes a buffer size adjustor which, based upon the corresponding cache performance, determines an optimum buffer size and assigns the optimum buffer size to the scalable buffer.

By contrast, Cheney relates to a system that manages the performance of a main memory, not a cache memory, through the use of a Spill Buffer in the main memory. As a matter of fact, Applicants have searched Cheney's specification and found no occurrence of the word "cache" or anything equivalent. While the Spill Buffer size may change, it varies only in accordance with parameters such as the operation modes and the frame sizes (Figs. 12-15) and there is no relationship or dependency between one and another Spill Buffer size. In other words, given a set of video decoding and displaying parameters, the Spill Buffer size is completely determined. Since Cheney does not teach a method of determining an optimal buffer size for a scalable buffer in accordance with the cache performance associated with a first and second buffer sizes, the Spill Buffer in Cheney is not equivalent to the scalable buffer in Applicants' invention.

As indicated in its title, Smith teaches a method of dynamically adjusting the sizes of a first and second portions of a cache memory in a data processing system wherein the first portion is allocated to storage of data blocks and the second portion is allocated storage of directory entries so as to minimize the sum of the expected cache miss rate and false invalidation rate. See, for example, column 3, line 51 - column 4, line 12. It is universally

understood by one skilled in the art that cache is a term in the art that always refers to a special type of memory device that operates significantly faster than the regular main memory. Put it another way, the present invention is directed toward the utilization of a scalable buffer within in a video decoder's main memory to optimize the video decoder's cache memory performance and the cache size remains constant during this optimization, while Smith's method directly manipulates a data processing system's cache memory size to strike a balance between the first portion storing data blocks and the second portion storing directory entries.

Figure 1 of the present application clearly demonstrates that caches 112, including data cache 113 and instruction cache 114, are distinct from data store buffers 160. The data store buffers 160 are ***scalable*** buffers utilized by the video decoding module 135 and the size of the data store buffers 160 is ***adjusted*** by the buffer size adjuster 152 and the cache 113's performance is ***analyzed*** by the analysis module 145 for different data store buffer sizes. See, for example, page 5, lines 10 - 29. Therefore, Smith does not teach a method of determining an optimum buffer size for a scalable buffer in the main memory based upon the corresponding cache memory performance.

Since Cheney and Smith, either alone or in combination, do not teach or suggest the use of a scalable buffer and the method of determining an optimum buffer size for the scalable buffer as recited in claim 13, claim 13 and its dependent claims 14 and 16-22 are patentable over Cheney in view of Smith.

Claim 1 is a method claim that has similar elements as claim 13. Therefore, claim 1 and its dependent claims 2-9 are also patentable over Cheney in view of Smith.

In addition, claims 8 and 21 recite that the size of video data stream processing instructions is modified according to the buffer size selected by the analysis module, and claims 9 and 22 further recite that the video data stream processing instructions are loop unrolled to match the buffer size selected by the analysis module.

Cheney, however, teaches the adjustment of a spill buffer to store picture ***data*** of different sizes, not video data stream processing ***instructions***. The video data stream processing instructions may be the same from one picture frame to another, whereas the picture data are dynamic all the time in a video stream.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 849-7721, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 15, 2004 _____ 31,066

Gary S. Williams (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
3300 Hillview Avenue
Palo Alto, California 94304
(650) 493-4935